Lesson 2

Digital Control of Three-Phase DC/AC Converters: Space Vector Modulation

Voltage Space Vector Modulation

• A three-phase inverter can generate three independent two-level phase voltages.
• Eight different instantaneous inverter configurations (states) are available.
• By suitably switching (modulation strategy) among these states it is possible to generate any triplet of average phase voltages \( V_{1\text{avg}} \), \( V_{2\text{avg}} \), \( V_{3\text{avg}} \) ranging from \( +E/2 \) to \( -E/2 \), where \( E \) is the DC link voltage.
Voltage Space Vector Modulation

- When the load is connected with insulated neutral, it is only sensitive to line-to-line voltages. The neutral voltage doesn’t have any effect on it.

- Any voltage triplet can be schematically represented as a vector laying on a plane (bi-dimensional representation). In general, the information about the value of the instantaneous neutral voltage (the third dimension!) cannot be represented and gets lost.
The voltage vector representing the triplet $v_1$, $v_2$, $v_3$, can be drawn by summing three vectors (length proportional to amplitude) directed as three 120° shifted axes (a, b, c).

We therefore defined a Direct Vector Transformation between the triplet $v_1$, $v_2$, $v_3$, and vector V. A similar transformation can be defined for inverter currents ....
**Voltage Space Vector Modulation**

The direct transformation can be analytically formulated referring to a couple of orthogonal axes \( \alpha \) and \( \beta \) (\( \alpha \) usually coincident with axis a).

\[
V_\alpha = V_1 - \frac{V_2}{2} - \frac{V_3}{2}
\]
\[
V_\beta = \frac{\sqrt{3}}{2}(V_2 - V_3)
\]

**Voltage Space Vector Modulation**

The reverse vector transformation can be achieved starting from a 2/3 V long vector and projecting it on the three axes a, b, c.

\[
V_1 = \frac{2}{3}V_\alpha
\]
\[
V_2 = \frac{2}{3}\left(\frac{\sqrt{3}}{2} V_\beta - \frac{V_\alpha}{2}\right)
\]
\[
V_3 = \frac{2}{3}\left(-\frac{\sqrt{3}}{2} V_\beta - \frac{V_\alpha}{2}\right)
\]
Voltage Space Vector Modulation

The inverter states can also be represented as voltage vectors. As an example:

State 100: \( V_1 = E \), \( V_2 = 0 \), \( V_3 = 0 \)

Voltage Space Vector Modulation

The zero vector can be generated in two equivalent ways:

State 111: \( V_1 = E \), \( V_2 = E \), \( V_3 = E \)

but also ...
Voltage Space Vector Modulation

State 000: $V_1=0$, $V_2=0$, $V_3=0$

- Space Vector Modulation (SVM) is performed by generating, within the switching period, a sequence of different inverter states.
- The sequence normally consists of three vectors, one of which is the zero vector.
- The durations of the three inverter states have to satisfy the following constraint:
  \[
  \delta_1 + \delta_2 + \delta_3 = 1
  \]
  where $\delta_i$ is the duty-cycle on phase $i$. 
Voltage Space Vector Modulation

- To generate a triplet $V_{1\text{avg}}, V_{2\text{avg}}, V_{3\text{avg}}$ (average voltages) in a switching period, vector $V^*$, the transformation of the triplet, is considered.

- The two adjacent vectors and a zero vector are applied successively.

Voltage Space Vector Modulation

- The projections of $V^*$ on the adjacent vectors determine the respective duty-cycles.

- The zero vector duty-cycle is determined from the relation:
  $$\delta_1 + \delta_2 + \delta_3 = 1,$$
  if possible.
Vectors $V^*$ which can be generated with this technique are the ones included in the hexagon [1].

It is possible to select different orders of application for the three vectors.

A possible vector sequence: we can do better than that ...
This choice reduces the number of switchings

This choice minimizes the current ripple’s amplitude
Voltage Space Vector Modulation

• The effect of the last strategy is to achieve centered voltage pulses. This is the same effect achieved with a conventional sine-triangle modulator having a 2T period.

• The difference is in the duty-cycles achieved cycle by cycle. With vector modulation an inherent third harmonic injection is implemented (the base vectors do not lay on the $\alpha$, $\beta$ plane).

• This allows the maximum modulation index to be equal to 1.15.
Voltage Space Vector Modulation
Neutral Voltage Variation

Voltage Space Vector Modulation
Third Harmonic Injection
By explicitly calculating [2] the instantaneous duty-cycles for pulse centered space vector modulation strategy, it can be demonstrated that the process is equivalent to conventional modulation where to all duty-cycle a common component is added, which is equal to:

\[-0.5 \times [ \max(\delta_1, \delta_2, \delta_3) + \min(\delta_1, \delta_2, \delta_3) ].\]

The waveform corresponding to the above relation is very close to a sinusoidal third harmonic. This also allows the maximum modulation index to be equal to 1.15.
Voltage Space Vector Modulation

- Another widely adopted modulation strategy is the so-called flat-top.
- A variable common component is added to each duty-cycle so that the modulation requires only two phases for each 60° interval of the fundamental period, while the third is not used (no switchings take place).
- The trick is to saturate the maximum (or minimum) duty-cycle in every switching period.
- This also allows the maximum modulation index to be equal to 1.15.
Voltage Space Vector Modulation

Instantaneous and average phase voltage with flat-top modulation. Each phase switches only in 2/3 of the fundamental period.

2E

V_{10}avg

V_{10}

0

Voltage Space Vector Modulation

Summing to each duty-cycle the same common component, constant or variable:

- the instantaneous phase voltages change;
- the average phase to neutral voltages change accordingly;
- the average phase to phase voltages do not change;
- if the neutral wire is insulated, the voltage on the load (Y) does not change.
Voltage Space Vector Modulation

- The calculations needed to implement the SVM concept are very effectively performed by means of μC and DSP’s.
- The pulse generation strategy adopted by the embedded PWM modulators is normally the one corresponding to minimum ripple.
- The SVM strategy is very widely used in modern digitally controlled three-phase VSI’s.

Digital Implementation of SVM

Modern μC’s and also some DSP’s greatly simplify the implementation of SVM:

- the PWM units automatically centre the pulses within the modulation period;
- the duty-cycles have to be provided to the PWM unit by a suitable algorithm;
- the direct implementation of Space Vector Modulation including α, β transform is often the preferred choice;
- sometimes post-processing of the duty-cycles can be adopted.
Digital Implementation of SVM

SVM is normally the inner routine in the digital control of a VSI; external current loops typically provide the set-point for the modulator:

- in the a, b, c fixed reference frame (the three duty-cycles are given);
- in the α, β fixed reference frame (bi-dimensional control: the average voltage vector components are given);

In the former case the duty-cycles can be modified by injecting a third harmonic component. The latter case is suited for direct SVM implementation.

Direct Implementation of SVM

- Given the α, β components of the set-point $V^*$, the digital modulator has to compute the projections of the reference vector $V^*$ on the adjacent inverter states.

- If a floating point processor is available, this is not a problem. If this is not the case, a lot of different algorithms can be applied. An example of SVM algorithm is reported in [3].

- Another example is described in the following.
Direct Implementation of SVM

- Some regularities in the transform matrixes $M_i$ can be exploited to rapidly calculate the $Z_{ix,y}$ components of the voltage vector $V^*$:

  \[
  \begin{align*}
  \text{tmp} &= V^*_\beta / \sqrt{3}; \\
  Z_{1x} &= V^*_\alpha - \text{tmp}; \\
  Z_{2y} &= -Z_{1x}; \\
  Z_{1y} &= 2 \cdot \text{tmp}; \\
  Z_{3x} &= Z_{1y}; \\
  Z_{2x} &= V^*_\alpha + \text{tmp}; \\
  Z_{3y} &= -Z_{2x};
  \end{align*}
  \]
Direct Implementation of SVM

• Once the \( Z_{ix,y} \) components of the voltage vector \( V^* \) are known it is easy to determine the sector \( V^* \) lies in, e.g.:

\[
\begin{align*}
Z_{1x} \cdot Z_{1y} &< 0 \ ? \\
&\begin{cases} 
yes & Z_{1x} > 0 \\
no & \end{cases} \\
Z_{2x} \cdot Z_{2y} &< 0 \ ? \\
&\begin{cases} 
yes & Z_{2x} > 0 \\
no & \end{cases} \\
Z_{3x} \cdot Z_{3y} &< 0 \ ? \\
&\begin{cases} 
yes & 1st \ 4th \\
no & 2nd \ 5th \\
\end{cases} \\
\end{align*}
\]

• Given the sector, it is immediate to determine which inverter voltage vectors have to be generated and consequently the required switching sequence.

• The durations of the two required inverter states \( V_1 \) and \( V_2 \) are proportional to the \( Z_{ix} \) and \( Z_{iy} \) components of the average vector \( V^* \) respectively.

• According to what was previously explained, the zero vector \( V_0 \) duration is given by the following:

\[
T_1 + T_2 + T_0 = T,
\]

unless saturation occurs.
Direct Implementation of SVM

• In the presence of saturation, i.e., when the required average voltage vector $V^*$ lies outside the hexagon, different strategies can be adopted.

• A possibility is to reduce the voltage vector $V^*$ amplitude, while keeping its phase, so as to put it on the hexagon border.

• This well exploits the inverter capability and is easy to implement:

$$T_{isat} = T \cdot T_i / (T_1 + T_2), \quad i = 1, 2$$

Direct Implementation of SVM

• A rough alternative which does not require troublesome calculations, is to reduce the smaller vector component enough to put the vector on the hexagon border:

• This solution implies an unavoidable error both in the amplitude and in the phase of the generated vector.
Direct Implementation of SVM

- If deep saturation occurs, i.e., at least one of the two components $V_k$ of vector $V^*$ is, by itself, outside the hexagon, another saturation strategy is normally adopted.
- The nearest inverter state is steadily generated for the complete switching period $T$.
- This leads the converter to six-step mode of operation.
- In the SVM algorithm the transition from light saturation to deep saturation can be suitably managed.

Light saturation areas

Deep saturation areas, extending also outside the circle
Final Remarks

• **SVM** is very commonly adopted in modern digital control of power converters (especially in drive applications).

• The implementation of SVM by means of μC’s or DSP’s is easy to achieve both directly (if the required computational power is available) and indirectly, by post-processing the phase duty-cycles with a suitable harmonic injection.

• In any case converter saturation must be considered and suitably dealt with.

References

