Digital Control Applications in Power Electronics

Simone Buso

University of Padova - Italy
Department of Electronics and Informatics
Power Electronics Laboratory

e-mail: simone@dei.unipd.it

Lesson 1

Digital Control Tools: Microcontrollers and Digital Signal Processors.
Introduction

Digital Control Advantages:
• Flexibility
• Ease of upgrade
• Man to Machine Interface (MMI)
• Sophisticated control techniques
• Reduced number of components
• Unsensitivity to components’ ageing ...

Digital Control Disadvantages:
• Design complexity
• Cost
• Dynamic performance (sampling frequency, quantization...)

Available tools for digital control implementation

• Microcontrollers (μC)
  ♦ CISC (Complex Instruction Set Computer) machines (micro-coded instructions)
  ♦ RISC (Reduced Instruction Set Computer) machines (with/without hardware multiplier)
  ♦ 4 to 32 bit CPU and bus

• Digital Signal Processors (DSP)
  ♦ Fixed-point arithmetic
  ♦ Floating-point arithmetic
Introduction

General μC features:

• specifically designed for control tasks
• A/D converters almost always included on chip
• capture and compare input pins available
• several programmable I/O pins
• timers and counters available (PWM)
• different kinds of external memory available (ROM, EEPROM, FLASH)
• different computational powers available (from 32 bit RISC to simple 8 bit CPU’s and even less)
• lots of third party development tools (EV-Boards, in-circuit emulators (ICE’s))

Introduction

General DSP features:

• not specifically designed for control tasks
• A/D converters not always included on chip
• useful peripheral units (CapCom, timers, PWM) normally not present on chip
• very high computational power available (32 bit RISC CPU’s both fixed and floating point)
• relatively few third party development tools (EV-Boards)
• new DSP solutions for power electronic applications are now becoming available (TMS320F240, ADMC401)
Microcontrollers

• A µC is essentially a computing machine where, on the same chip, a CPU core is interfaced with different peripheral units, allowing it to perform various control functions.

• In modern µC’s, the typical CPU architecture is the so-called Harvard architecture, based on separate program and data memories and buses. An hardware multiplier is quite often present in state of the art products.

• The typical peripheral units include:
  ♦ A/D converters
  ♦ Timers and counters
  ♦ PWM modulators

In the selection of a µC unit for any given control application some key parameters must be considered:

• performance parameters
• cost parameters

As in any project, these two aspects typically have to be traded-off.
Microcontrollers

Typical performance parameters are:

- CPU clock period
- instruction cycle
- instruction set (RISC or CISC)
- memory area
- interrupt management
- peripheral unit availability

The cost is indirectly determined also by:

- availability of development tools
- cost of the evaluation board, ICE, etc. etc.

and strongly depends on production volume

Microcontrollers

- The μC market is very large and rich of products. A lot of manufacturers offer complete sets of μC solutions, with increasing complexity, level of performance and cost.

- An exhaustive overview is practically impossible; some examples can be shown of different products with different complexities, which allow to get a glimpse of what can be found on the market.

- Common features in terms of system architecture and peripheral units can be easily identified.
Example: ST6 microcontroller [1]

- Very simple (16 pins) and low cost µC, with 8-bit CPU and 9 I/O pins.
- Low supply voltage (3V, 6V).
- Low clock frequency (8Mhz max.)
- Minimum instruction cycle 1.625µs.
- Low computational power: only 40 simple instructions are available (no multiply instruction).
- Peripheral units limited to Timer and A\D converter (8 bit).
- Typical applications: sequence control, display driver, simple and low speed closed loop controls.

ST6 microcontroller block diagram
ST6 microcontroller

CPU block diagram

Example: Siemens 8xC166 µC [2]

- Typical (but not widely used) 16-bit µC.
- High clock frequency (20MHz maximum (internal)).
- RISC machine with a large majority of single-cycle instructions (100ns) thanks to an internal pipeline.
- Von Neumann architecture (a single memory space is used both for data and program code).
- Medium computational power (no hardware multiplier).
- Available peripheral units:
  - 2 general purpose timers 16 bit;
  - 2 independent serial communication channels;
  - 10 channels, 10-bit, 10 µs A/D converter;
  - 16 capture and compare (CAPCOM) channels.
Siemens 8xC166 series overview

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Type Code</th>
<th>Memory Type Code</th>
<th>Memory Designation</th>
<th>Memory Size Code</th>
<th>Package Code</th>
<th>Temp. Range Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROMLess</td>
<td>80</td>
<td>SAB</td>
<td>C166</td>
<td>(-)</td>
<td>M</td>
<td>0° / 70°</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>C166W</td>
<td>(-)</td>
<td>M</td>
<td>-40° / 85°</td>
</tr>
<tr>
<td>Metal Mask ROM</td>
<td>83</td>
<td>SAB</td>
<td>C166</td>
<td>5</td>
<td>M</td>
<td>0° / 70°</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>C166W</td>
<td>5</td>
<td>M</td>
<td>-40° / 85°</td>
</tr>
<tr>
<td>Flash EEPROM</td>
<td>88</td>
<td>SAB</td>
<td>C166</td>
<td>5</td>
<td>M</td>
<td>-40° / 110°</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>C166W</td>
<td>5</td>
<td>M</td>
<td>0° / 70°</td>
</tr>
</tbody>
</table>

**SAB 80C166 Block Diagram**

- CPU CORE
- Dual Port RAM 1 KByte
- Interrupt Controller
- Watchdog
- External Instr./Data
- External Bus Controller
- 10-Bit ADC
- USART
- ASC
- BRG

**Siemens 8xC166 series overview**

- W = without prescaler
- M = Metal Quad Flatpack
- (-) no suffix

**SAB 80C166 Block Diagram**

- Up to 32 KByte ROM: Flash EPROM
- OSC
- External Input Data
- External Output Data
- PEC
- Interrupt Bus
**SAB 80C167 Block Diagram**

**Peripherals Set of the SAB 80C167**

- **2 General Purpose Timer units (GPT1 & GPT2)**
  - 5 Timers (200/400ns) with multiple Input/Output, Reload and Capture functions and complex concatenation capabilities
- **Capture/Compare unit (CAPCOM)**
  - 2 timers (400ns) each with Reload register and 16 independent 16-bit Capture/Compare channels programmable to 6 modes of operation
- **4 high resolution PWM channels**
  - with independent time-base of up to 50ns resolution and programmable operation modes
- ...
Peripherals Set of the SAB 80C167

- Fast and accurate A/D Converter
  - 10-bit resolution, 10 input channels, 9.7µs conversion time, continuous and scan modes
- I/O Ports
  - 8 ports provide 111 I/O lines
- Watchdog: 16-bit Reload-timer causes reset on overflow
- 2 independent identical USARTs
  - max 625Kbaud asynchronous
  - max 2.5Mbit/sec synchronous data transfer

Pulse Width Modulation Unit (PWM)

- 4 completely independent PWM channels each with its own time-base
  - 50ns or 12.8µs timer-resolution provides a very wide frequency range to generate PWM signals
  - Programmable output polarity
  - Up to 78 KHz at 8-bit PWM resolution
  \[
  F_{PWM} = \frac{1}{2^{8 \times 50ns}} = 78 \text{ KHz}
  \]
- Four operation modes
  - Standard, edge-aligned PWM
  - Symmetrical, center-aligned PWM for asynchronous motor control
  - Burst-mode for modulated PWM signals
  - Single-shot mode
Pulse Width Modulation Unit (PWM)

PMW Unit Frequencies and Resolution in Mode 0 Operation (EDGE-ALIGNED)

<table>
<thead>
<tr>
<th>Resolution</th>
<th>8 Bit</th>
<th>10 Bit</th>
<th>12 Bit</th>
<th>14 Bit</th>
<th>16 Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Clock (50ns Resolution)</td>
<td>78.1 KHz</td>
<td>19.5 KHz</td>
<td>4.88 KHz</td>
<td>1.22 KHz</td>
<td>305 Hz</td>
</tr>
<tr>
<td>CPU Clock / 64 (3.2µs Res.)</td>
<td>1.22 KHz</td>
<td>305 Hz</td>
<td>76.3 Hz</td>
<td>13.1 Hz</td>
<td>4.77 Hz</td>
</tr>
</tbody>
</table>

PMW Unit Frequencies and Resolution in Mode 1 Operation (SYMMETRICAL)

<table>
<thead>
<tr>
<th>Resolution</th>
<th>8 Bit</th>
<th>10 Bit</th>
<th>12 Bit</th>
<th>14 Bit</th>
<th>16 Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Clock (50ns Resolution)</td>
<td>39.1 KHz</td>
<td>9.77 KHz</td>
<td>2.44 KHz</td>
<td>610 Hz</td>
<td>152.6 Hz</td>
</tr>
<tr>
<td>CPU Clock / 64 (3.2µs Res.)</td>
<td>610 Hz</td>
<td>152.6 Hz</td>
<td>38.15 Hz</td>
<td>9.54 Hz</td>
<td>2.4 Hz</td>
</tr>
</tbody>
</table>

PWM unit Mode 0 and 1...

PWM Mode 0: Standard PWM’s or Edge-Aligned PWM’s

- Timer Period
- Contents of the Period Register (PPx)
- PWM Signal
- Contents of the PWx Register
- Interrupt Request and Latch of the Shadow Register

If all channels are programmed to mode 0, edge-aligned PWM signals will be generated. A duty cycle from 0 to 100% is programmable

PWM Mode 1: Symmetrical or Center-Aligned PWM’s

- Timer Period
- Contents of the PWx Register
- PWM Signal
- IR and Latch of the Shadow Register

If all channels are programmed to mode 1, center-aligned PWM signals will be generated. A duty cycle from 0 to 100% is programmable
### PWM unit Mode 0 and 1

**Burst Mode:** Burst Sequence by combining PWM channel 0 and 1

**Single Shot:** Only one PWM Pulse is generated Mode available for channel 2 and 3

- **Output Result:** Channel 1 is modulated by Channel 0
- **The Timer can be dynamically changed to lengthen (retrigger) or shorten the output pulse**

### Example: Hitachi H8S series [3]

- **Recent** 16-bit µC (evolution of H8/500 series).
- **High clock frequency** (20MHz and higher).
- **Single cycle instructions** (200ns @20MHz).
- **Rich set of instruction** (CISC machine).
- **Hardware multiplier and accumulator** for DSP-like applications.
- **Medium/high computational power**.
- **Available peripheral units:**
  - timer unit for CAPCOM or PWM functions
  - serial communication interface
  - 8 channel, 10-bit, 1 µs A\D converter
  - 2 channel, 10µs D\A converter (only in some versions)
Example: Microchip PIC17C7xx [4]

- State of the art 16-bit μC (5V supply, stand-by current < 1μA).
- High clock frequency (33MHz maximum).
- Single cycle instructions (121ns @33MHz).
- RISC machine (58 single-word 16-bit instructions).
- Modified Harvard architecture with hardware multiplier.
- High computational power.
- Available peripheral units:
  - 4 timers 8-16 bit;
  - serial communication interface;
  - 12-16 channels, 10-bit, 16 μs A\D converter;
  - 3 PWM 10 bit outputs.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>PIC17C76A</th>
<th>PIC17C78A</th>
<th>PIC17C76B</th>
<th>PIC17C76C</th>
<th>PIC17C78B</th>
<th>PIC17C78C</th>
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<tbody>
<tr>
<td>Maximum Frequency of Operation</td>
<td>33 MHz</td>
<td>33 MHz</td>
<td>33 MHz</td>
<td>33 MHz</td>
<td>20 MHz</td>
<td>20 MHz</td>
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<tr>
<td>Operating Voltage Range</td>
<td>3.3 V - 5.5 V</td>
<td>3.3 V - 5.5 V</td>
<td>3.3 V - 5.5 V</td>
<td>3.3 V - 5.5 V</td>
<td>2.7 V - 5.5 V</td>
<td>2.7 V - 5.5 V</td>
</tr>
<tr>
<td>Program Memory (KB)</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>Data Memory (KB)</td>
<td>256</td>
<td>256</td>
<td>256</td>
<td>256</td>
<td>512</td>
<td>512</td>
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<td>External Interrupt Sources</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>5</td>
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<tr>
<td>Watchdog Timer</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>General Timers</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Power-on Reset</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>ISP Support</td>
<td>8.25 ms</td>
<td>8.25 ms</td>
<td>8.25 ms</td>
<td>8.25 ms</td>
<td>8.25 ms</td>
<td>8.25 ms</td>
</tr>
<tr>
<td>Package Types</td>
<td>40 I/O</td>
<td>40 I/O</td>
<td>40 I/O</td>
<td>40 I/O</td>
<td>40 I/O</td>
<td>40 I/O</td>
</tr>
</tbody>
</table>

Note: Pins P1A and P1B can sink up to 60 mA

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**CPU**

**Microchip PIC17C7xx**

**Data memory**

**Program memory**

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Lesson #1
Example: Hitachi SH7000 Series [3]

- State of the art 32-bit μC (5V or 3.3V supply).
- High clock frequency (28MHz @ V<sub>cc</sub> = 5V).
- RISC machine (61 single-word 16-bit instructions).
- Single cycle instructions (35ns) thanks to internal five-stage pipeline.
- Modified Harvard architecture with hardware multiplier (MAC: 32x32 bit, 64 bit → 64 bit).
- High computational power.
- Available peripheral units:
  - 16 bit, 5 channels multifunction timer unit (PWM);
  - 16 bit, 2 channel compare and match;
  - 8 channels, 10-bit, 2.9 μs, A/D converter;
  - watchdog timer.

![SH7040 A/D converter](image)
Digital Signal Processors [5]

First development in the late 70’s (TMS320C10 - 1979). Typically designed for open loop digital signal processing e.g.:

- real time FFT calculation;
- digital filtering of sampled signals.

The market for this kind of applications is enormous (10 billion US$/year) and is steadily growing, including telecom and consumer electronics.

Applications in industrial electronics (control tasks) are rather insignificant in volume. The manufacturers offer very few control oriented solutions.

Digital Signal Processors

Two types of DSP’s can be found:

- fixed point DSP (16, 24 bit);
- floating point (typically 32 bit or more).

For control applications, fixed point DSP’s are very close to modern top-level µC’s (RISC machines with Harvard architecture and hardware multiplier) in terms of performance. They are normally much less effective in terms of peripherals. Globally, they appear more expensive.

Floating point DSP’s are very advantageous, but only for those applications where high cost for the control system can be afforded. The lack of peripheral units is almost total (⇒ you must add them).
Digital Signal Processors

Schematic diagram of a DSP with Harvard architecture.

Parallel processing of instructions and data is allowed by multiple bus architecture.

The instruction processor takes care of address computations.

Modern DSP’s normally adopt modified Harvard architectures featuring:

- improved instruction processors with more than a single address generator;
- improved processing units with multiple independent logic units (ALU, MAC, SHIFT);
- application specific hardware modules (e.g. registers, timers etc.) in the CPU to speed-up typical calculations (e.g. DFT);
- different internal memory structures with multiple data memories and buses or mixed program and data memories (useful for filter coefficients).
Example: Analog Devices ADSP2186 [5]

- State of the art fixed point DSP.
- 25 ns instruction cycle for 40 MIPS performance.
- Single-cycle instruction execution.
- Single-cycle context switch.
- 3-bus architecture for dual operand fetch in every instruction cycle.
- Dual address generator.
- Independent ALU, MAC and SHIFTER units.
- 40 kbyte on chip RAM.
- Dual purpose program memory allowing both instruction and data storage.

Example: Analog Devices ADSP2186

1: Address Bus
2: Data Bus
3: Internal Result Bus
Example: Analog Devices ADSP2186

A very high level of parallelism is achieved by means of multiple processing units, multiple buses and complex address generators. In a single cycle the DSP can:

• generate the next program address;
• fetch the next instruction;
• perform one or two data moves;
• update one or two data address pointers;
• perform a computational operation.

The program sequencer allows conditional jumps, subroutine calls and returns in a single cycle.

Example: Analog Devices ADSP21060 [5]

• State of the art floating point DSP.
• 25 ns instruction cycle for 40 MIPS performance.
• Single-cycle instruction execution.
• 32 bit single precision and 40 bit extended precision IEEE floating point data format (24 bit mantissa 8 bit exponent / 11 bit exponent) or 32 bit fixed point data format.
• 48 bit instruction word for various parallel operations.
• 4 independent buses for dual data fetch, instruction fetch and I/O (super-Harvard architecture).
• 3 independent 32 bit floating point computational units.
• Specific instructions for accelerated FFT computation.
**Example: Analog Devices ADSP21060 [5]**

![Diagram of Analog Devices ADSP21060](image)

**New DSP solutions**

Recently, new DSP solutions have been proposed by some manufacturers which merge the DSP computational capabilities with some typical μC peripheral units.

The idea is to provide the designer with a control oriented DSP, allowing the direct implementation of closed loop digital control of power converters with minimum additional interface circuitry.

The main advantage with respect to any μC is in the very high computational capability of the DSP.

Since these devices are not very popular yet, the cost factor may be their weak point.
Example: Analog Devices ADMC401 [5]

- **Fixed-point DSP core features:**
  - 26 MIPS performance;
  - ADSP 21xx compatible;
  - Single cycle instruction execution (38.5 ns @ 13 MHz clock frequency);
  - 16 bit arithmetic and logic unit;
  - Single Cycle 16 bit X 16 bit MAC.

- **Built-in peripheral units:**
  - High resolution multi-channel ADC;
  - Three-phase 16 bit PWM generation unit;
  - dual channel event timer unit (CAPCOM);
  - Incremental encoder interface unit.

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Example: Analog Devices ADMC401

**Functional Block Diagram**
ADMC401: Analog to Digital Converter

- 8 analog inputs.
- 12 bit resolution.
- conversion time: 2 µs (all channels thanks to four stage pipeline architecture).
- 4 V p-p input voltage range
- 2 channels can be simultaneously sampled.
- conversion can be synchronized to PWM or externally triggered.

ADMC401: PWM Generation Unit

- 6 PWM outputs.
- 16 bit counter resolution.
- programmable output polarity.
- static or chopped output signals.
- programmable dead-time and minimum pulse width.
- single update and double update mode (for asymmetrical PWM patterns).
- switching frequency from 198 Hz to 102 kHz.
ADMC401: Incremental Encoder Interface

- 16 bit up-down counter (frequency and direction of rotation detection).
- Programmable input noise filter (to avoid spurious triggering).
- Two additional strobe inputs (to latch the counter contents into registers).
- 16 bit loop timer (position and speed loops set point generation).

ADMC401: Event Timer Unit

- 16 bit dedicated timer with programmable frequency.
- 2 independent channels.
- 2 programmable (rising edge or falling edge) events for each channel.
- Single shot and free-running modes of operation.
- Only capture function, no possibility of compare mode.
ADMC401: Other Ancillary Functions

- 2 auxiliary 8 bit PWM timers
- 16 bit watchdog timer
- Programmable digital I/O port (12 pin)
- 2 synchronous serial ports

Example: Texas Instruments TMS320F240 [6]

- Fixed-point DSP core features:
  - 20 MIPS performance;
  - TMS320C25 source code compatible;
  - Single cycle instruction execution (50 ns @ 20 MHz CPU clock frequency);
  - 16 bit arithmetic and logic unit;
  - Single Cycle 16 bit X 16 bit signed product.

- Main built-in peripheral units:
  - 10 bit resolution, 16 channel ADC;
  - 12 channel 16 bit PWM generation unit;
  - 3 16 bit general purpose timers;
  - 4 independent capture circuits.
TMS320F240 Functional Block Diagram

- Central Arithmetic Logic Unit (CALU)
- Event Manager: Timers
- Compare Units...
- Dual 10 bit ADC

TMS320F240 Central Arithmetic and Logic Unit

- Advanced Harvard architecture with multiple bus.
- 16 bit X 16 bit hardware multiplier with 32 bit accumulator (1 cycle execution).
- 16 bit input scaling shifter (used for data alignment before logic or arithmetic operations).
TMS320F240 Event Manager

- 3 general purpose timers for 16 bit up/down counts and compare functions (including additional PWM generation).
- 6 full compare outputs for PWM applications with dead-time generators (0 to 102μs).
- 3 simple compare units.
- The 12 available PWM outputs have all 50 ns resolution and 16 bit dynamic range.
- 4 channel capture unit operating on GPT1 or GPT2, with 2 level FIFO.

TMS320F240 Analog to Digital Converter

- 2 10 bit ADC’s with built-in S/H circuits.
- 16 input channels available, but only 2 can be sampled simultaneously.
- Minimum conversion time 6.1 μs.
- Single shot or continuous mode of operation.
- 2 level FIFO for result storing.
TMS320F240 Ancillary Peripheral Functions

- 4 pin serial peripheral interface
- watchdog timer
- Quadrature - encoder pulse circuit
- 28 programmable I/O pins

References