High Step-up Ratio DC-DC Converter Topologies

Part II

Speaker: G. Spiazzi

P. Tenti, L. Rossetto, G. Spiazzi, S. Buso, P. Mattavelli, L. Corradini
Dept. of Information Engineering - DEI
University of Padova
Seminar Outline

• Why we need high step-up ratio converters?
  - Application fields

• Low power high step-up ratio topologies
  - Coupled inductors

• High power high step-up ratio topologies
  - Non isolated
  - Isolated
Cascaded Boost Converter

Voltage conversion ratio: \[ M = \frac{U_o}{U_g} = \frac{U_o}{U_1} \frac{U_1}{U_g} = \frac{1}{1-d_1} \frac{1}{1-d_2} \]

- Reduced \( S_1 \) and \( D_1 \) voltage stress
- High flexibility
- Suitable for high power applications through interleaving connections
- Total power processed twice
- High \( S_2 \) and \( D_2 \) voltage stress
Voltage multiplier cell

- Reduced switch and diode voltage stress ($U_{DS} \approx U_o/2$)
- ZCS and soft diode turn off through the use of a resonant inductor $L_r$
- Suitable for high power applications through interleaving connections
- Maximum and minimum duty-cycle limitation to guarantee soft commutations
- High switch RMS current
- Voltage stress reduction related to the number of cells

Voltage conversion ratio:

$$M = \frac{U_o}{U_g} \approx \frac{2}{1 - d}$$
Boost with Voltage Multiplier Cells

Voltage conversion ratio:

$$M = \frac{U_o}{U_g} \approx \frac{M+1}{1-d}$$

Switch voltage stress:

$$U_{DS} \approx \frac{U_o}{M+1}$$
Converter Operation (CCM)

\[ T_{01} = t_1 - t_0 \]
Converter Operation (CCM)

\[ T_{12} = t_2 - t_1 \]
Converter Operation (CCM)

\[ T_{23} = t_3 - t_2 \]

Soft \( D_{m1} \) turn off
Converter Operation (CCM)

\[ T_{34} = t_4 - t_3 \]

Soft D turn off
Converter Operation (CCM)

\[ T_{45} = t_5 - t_4 \]

Soft \( D_{m2} \) turn off
Dual Boost Converter

Voltage conversion ratio:

\[ M = \frac{U_o}{U_g} = \frac{1 + d}{1 - d} \]

Output voltage of each converter:

\[ M_1 = \frac{U_1}{U_g} = M_2 = \frac{U_2}{U_g} = \frac{1}{1 - d} \]
Dual Boost Converter

↑ Reduced switch and diode voltage stresses
↑ Inductor $L_1$ and $L_2$ rated roughly at half of total input current
↑ Suitable for high power applications through interleaving connections of each module
↓ Need for isolated gate driver
↓ Floating load connection
↓ Limited switch voltage stress reduction
↓ Penalty in the converter efficiency (negligible for high conversion ratios)
Dual Boost Converter

Power processed by each module:

\[ P_1 = U_1 I_0 = P_2 = U_2 I_0 = P \]

Efficiency of each module:

\[ \eta_1 = \frac{P_1}{P_g} = \frac{P_1}{P_1 + P_d} \]

Efficiency reduction:

\[ \eta_T = \frac{P_0}{P_g} = \frac{P_0}{P_0 + 2P_d} = \frac{(U_1 + U_2 - U_g)I_0}{(U_1 + U_2 - U_g)I_0 + 2P_d} = \frac{2P - U_g I_0}{2(P + P_d) - U_g I_0} \]

\[ \eta_T = \frac{1 - \frac{1}{2M_1}}{\eta_1} = \frac{2M_1 - 1}{2M_1 - 1} = \frac{M}{M+1} - 1 = \frac{\eta_1 M}{M+1 - \eta_1} \]
Dual Boost Converter

Efficiency reduction: \[ \eta_T = \frac{\eta_1 M}{M + 1 - \eta_1} \]
Interleaved Boost with Voltage Multiplier

- Reduced switch and diode voltage stress ($U_o/2$)
- Inductor $L_1$ and $L_2$ rated at half of total input current
- Reduced input current ripple due to interleaved operation
- Voltage multiplier cell operation requires $d > d_{\text{min}}$
- More ringing on switch voltage due to capacitor ESL

Voltage conversion ratio $d > 0.5$:

$$M = \frac{U_o}{U_g} = \frac{2}{1 - d}$$
Current Waveforms $d > 0.5$

$U_1 = U_2 = \frac{U_o}{2}$
Interleaved Boost with Voltage Multiplier

\[ U_g = 20V, P_g = 1280W, U_o = 400V, P_o = 1080W \]

Unbalance due to slightly different switch on times
Interleaved Boost with Voltage Multiplier

$U_g = 20V$, $P_g = 1280W$, $U_o = 400V$, $P_o = 1080W$

**Effect of capacitor ESL and layout parasitic inductances**
Boost with Voltage Doubler

Voltage conversion ratio $d > 0.5$:

Similar behavior as the interleaved boost with voltage multiplier

Problem: for $d < 0.5$ the switch voltage stress ($S_1$) becomes the output voltage
Extension to Higher Step-up Ratios

\[ U_2 = \frac{U_3}{2} = \frac{U_0}{3} \]

Voltage conversion ratio \( d > 2/3 \):

\[ M = \frac{U_0}{U_g} = \frac{3}{1 - d} \]
Boost with Voltage Doubler

Interleaved boost with voltage multiplier versus Boost with voltage doubler

Similar behavior for duty-cycle higher than 50% but the structure becomes asymmetric
Boost with Three-state Switching Cell

Voltage conversion ratio (d > 0.5):

\[ M = \frac{U_o}{U_g} = \left( \frac{n+1}{n} \right) \frac{1}{1-d} \]

\[ n = \frac{N_p}{N_s} \]

↑ Reduced switch and diode voltage stress (depending on n)
↑ Reduced input current ripple due to interleaved operation
↓ Voltage multiplier cell operation requires d > d_{min}
↓ Correct operation requires \( L_{\mu} > L_{\mu_{min}} \)
↓ Operation modes with very low gain
Boost with Three-state Switching Cell

Voltage conversion ratio

\[ u_2 = u_3 \approx 0 \]

DCM operation with very low gain
Interleaved Boost with Coupled Inductors and Voltage Multiplier

Voltage conversion ratio \( d > d_{\text{min}} \) (CCM):

\[
M = \frac{U_o}{U_g} \approx \left( \frac{n + 2}{n} \right) \frac{1}{1 - d}
\]

\[
n = \frac{N_p}{N_s} \quad \frac{L_m}{L_m + L_d} \approx 1
\]

Normalized switch voltage stress:

\[
U_{\text{swN}} = \frac{U_{\text{sw}}}{U_o} = \frac{U_3}{U_o} \approx \frac{n}{n + 2}
\]
Interleaved Boost with Coupled Inductors and Voltage Multiplier

Voltage conversion ratio $d \geq d_{\text{min}}$ (CCM):

$$M = \frac{U_o}{U_g} \approx \left( \frac{n + 2}{n} \right) \frac{1}{1 - d}$$

$$n = \frac{N_p}{N_s} \frac{L_m}{L_m + L_d} \approx 1$$

↑ Reduced switch and diode voltage stress (depending on $n$)
↑ Reduced input current ripple due to interleaved operation
↑ No reverse recovery losses (ZCS turn on)
↓ Voltage multiplier cell operation requires $d > d_{\text{min}}$
↓ High switch current stress
Operation for $d > d_{\text{min}}$ (CCM)

$T_{01} = t_1 - t_0$
Operation for $d > d_{\text{min}}$ (CCM)

\[ T_{12} = t_2 - t_1 \]
Operation for $d > d_{\text{min}}$ (CCM)

$T_{23} = t_3 - t_2$

$S_1$ ZC turn on
Operation for $d > d_{\text{min}}$ (CCM)

$T_{34} = t_4 - t_3$

Soft $D_1$ turn off
Operation for $d > d_{\text{min}}$ (CCM)

$T_{45} = t_5 - t_4$
Operation for $d > d_{\text{min}}$ (CCM)

$\mathbf{T}_{56} = t_6 - t_5$

Soft $D_4$ turn off
Operation for $d > d_{\text{min}}$ (CCM)

$T_{67} = t_7 - t_6$
Operation for $d > d_{\text{min}}$ (CCM)

$S_2$ ZC turn on

$T_{78} = t_8 - t_7$
Operation for $d < d_{\text{min}}$ (CCM)

Voltage conversion ratio $d < d_{\text{min}}$ (CCM):

$$M = \frac{U_o}{U_g} \approx \frac{1}{1 - 2d}$$

$$n = \frac{N_p}{N_s} \quad \frac{L_m}{L_m + L_d} \approx 1$$

- The multiplier cell is disabled ($u_1 = u_2 \approx 0, U_3 \approx U_o$)
- The switch voltage stress becomes equal to the output voltage
- The magnetizing currents are in phase
Voltage Conversion Ratio (CCM)

\[ \frac{1}{1 - 2d_{\text{min}}} = \frac{n + 2}{2} \frac{1}{1 - d_{\text{min}}} \]

\[ d_{\text{min}} = \frac{2}{n + 4} \]

- Disabled multiplier cell
- \( n = 0.5 \)
- \( n = 0.7 \)
- \( n = 1 \)
Minimum Switch Voltage Stress

Normalized switch voltage stress for \( d = d_{\text{min}} \):

\[
U_{\text{sw}1N} = \frac{U_{\text{sw}}}{U_o} \approx \left( \frac{1}{1 - 2d_{\text{min}}} \right) \frac{1}{M}
\]

\[
= \frac{n + 4}{nM}
\]

Normalized switch voltage stress at nominal conditions (\( d > d_{\text{min}} \)):

\[
U_{\text{sw}2N} = \frac{U_{\text{sw}}}{U_o} \approx \frac{n}{2 + n}
\]

Optimum turns ratio:

\[
U_{\text{sw}1N} = U_{\text{sw}2N}
\]

\[
n_{\text{opt}} = \frac{3}{M - 1} \left( 1 + \sqrt{1 + \frac{8}{9} (M - 1)} \right)
\]
Minimum Switch Voltage Stress

\( U_{\text{swNmin}} \)

- 0.5
- 0.45
- 0.4
- 0.35
- 0.3
- 0.25

- 5
- 7
- 9
- 11
- 13
- 15
- 17
- 19
- 21
- 23
- 25
Isolated Interleaved High Gain Converter

- Reduced switch and diode voltage stress
- Reduced input current ripple due to interleaved operation
- No reverse recovery losses (ZVS-ZCS switch turn on)
- Same operation mode independent of duty-cycle value
- High switch and winding current RMS value
Main Waveforms

\[ T_{01} = t_1 - t_0 \]
Main Waveforms

\[ T_{12} = t_2 - t_1 \]

S3 ZV & ZC turn on
Main Waveforms

\[ T_{23} = t_3 - t_2 \]

\[ S_1 \text{ ZV & ZC turn on (} i_1 \text{ is negative when } S_3 \text{ turns off) } \]
Main Waveforms

\[ T_{34} = t_4 - t_3 \]

Soft D₁ turn off (no reverse recovery problem)
Main Waveforms

$S_4$ ZV & ZC turn on

$T_{45} = t_5 - t_4$
Main Waveforms

$S_2$ ZV & ZC turn on
($i_2$ is negative when $S_4$ turns off)

$T_{56} = t_6 - t_5$
Main Waveforms

Soft $D_2$ turn off
(no reverse recovery problem)

$T_{01} = t_1 - t_2$
Mismatch Sensitivity

- In case of parameter and/or duty-cycle mismatch between the interleaved boost sections severe current mismatch occurs.
- The solution is to employ individual clamp capacitors for each subsection (in this case, the mismatch is absorbed by a small difference between the clamp capacitor voltages).
Different operation mode is achieved by reducing the capacitor value of the voltage multiplier cell.

Half-cycle resonances occur between capacitor $C_1$ and $C_2$ and transformer leakage inductances $L_d$. 

Resonant capacitors
Main Waveforms

<table>
<thead>
<tr>
<th></th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$D_1$</th>
<th>$D_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{01} = t_1 - t_0$</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>$T_{12} = t_2 - t_1$</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>$T_{23} = t_3 - t_2$</td>
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</tbody>
</table>

Hard $S_1$ and $S_2$ turn on

Soft $D_1$ and $D_2$ turn off

ZV & ZC turn on of $S_3$ and $S_4$
Preliminary Experimental Results

\[ U_g = 35V, U_o = 360V, P_o = 2500W, f_{sw} = 40kHz \]

High voltage ripple on clamp capacitors

Current waveform is half way between non resonant and resonant behaviors
Conclusions

• For high power applications, high step-up converters working with a quite high input current value should have a continuous input current absorption.
• Interleaved operation at input side helps to reduce the input current ripple as well as to share the total input current between different conversion subsections.
• A voltage multiplier at the output side avoids the use of dissipative snubbers across the output diodes.
• Isolated structures operate in the same manner independent of the duty-cycle value (they are better than the non-isolated ones)